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(54) Title: NEW DESIGN STRUCTURES OF AND SIMPLIFIED METHODS FOR FORMING FIELD EMISSION MICROTIP ELECTRON EMITTERS

(57) Abstract: Electron emission structures formed using standard semiconductor processes on a substrate first prepared with a topographical feature are disclosed. At least one layer of a first material is concurrently deposited on the substrate and etched from the substrate to form an atomically sharp feature. An at least one layer of a second material is deposited over the atomically sharp feature. A conductive layer is deposited over the at least one layer of the second material. A selected area of material is removed from the conductive layer and the at least one layer of second material to expose the atomically sharp feature. Finally, electrical connectivity is provided to elements of the electron emission structure.

NEW DESIGN STRUCTURES OF AND SIMPLIFIED METHODS FOR FORMING FIELD EMISSION MICROTIP ELECTRON EMITTERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to semiconductor devices, and in particular, relates to topographic features of semiconductor devices.

2. Background Information

Semiconductor fabrication techniques usually involve multi-step processes. Some multi-step processes are very expensive because different fabrication techniques or materials are required for each process step. Additionally, the fabrication process for one material might be incompatible with another process due to cross-contamination by dopants or etching materials. Devices created with single-crystal silicon, for example have a much lower yield and a higher failure rate than anisotropic silicon devices. The high heat required for some single-crystal fabrication excludes processing at the end of a manufacturing cycle. Therefore, it is difficult to form devices of high quality and uniformity using single-crystal materials or to combine production of such devices with other semiconductor fabrication processes.

One use of single-crystal semiconductor fabrication is the formation of atomically sharp topographies. Atomically sharp topographies are generally formed using crystallographic etched monolithic films of tungsten, silicon, or diamond-like films. The processes used to create atomically sharp topographies using single-crystal fabrication cannot easily be combined with other semiconductor processes due to high temperatures and other constraints. Atomically sharp topographies are very desirable for several applications.

One use for an atomically sharp object is a field emission structure. Field emission structures are well known in the art and include devices such as field emission microtip electron emitters, area emitters, and Field Effect Transistors (FETs). The term "field emission microtip electron emitter" is interchangeable with Field Emission (FE) electron emitter, microtip emitter, cold-cathode tip emitter, Spindt tip emitter, field tip emitter and tip emitter. The field emission electron emitter is a field effect device that emits charged particles when a voltage potential is applied in a particular manner. The charged particle

emissions may be controlled by changing the potential voltage with respect to regions of the device. In general, a *microtip field emitter* has several components including a substrate or base, an atomically sharp feature known as a tip, emitter tip or microtip, and a bias plane. Fabrication of the atomically sharp emitter microtip has generally required the use of single-crystal materials. There are a number of techniques for creating atomically sharp topographies on a substrate for use in a field emission structure.

Field emission electron emitters are usually formed using photolithographic and lift-off techniques to form atomically sharp topographic features on a monolithic film. The methods used to form emitter microtips include molding, electro-etching and thermal oxidation. An example of several methods for creating field emission emitters.

Figure 1 is an illustration of a technique for creating microtip emitters. The technique is attributed to the French national laboratory, Laboratoire d'Electronique de Technologie et d'Instrumentation (LETI), and illustrates a method of forming what are generally known as Spindt emitters after Dr. Capp Spindt of the Stanford Research Institute.

Figure 2 is an illustration of a technique for creating a microtip. The technique of Henry Gray relies on an etched silicon mold that is subsequently used as a mold for a metal microtip. A substrate of silicon crystal is etched using an anisotropic etching process to form a pyramidal pit to be used as a mold. The silicon mold is deposited with a metal layer then silicon mold is etched away leaving the metal layer with an atomically sharp microtip.

Figure 3 is an illustration of a technique for creating microtip emitters. The technique of Henry Gray applies the microtip of Figure 2 to form microtip emitters. Figure 4 is an illustration of a technique for creating microtip emitters. The technique of J. Itoh et al, of Electrotechnical lab Ibarake, Japan, utilizes a tetrode structure to form microtip emitters.

Figure 5 is an illustration of a technique for creating microtip emitters. The technique of Kanamaru et al of Electrotechnical lab Ibarake, Japan, utilizes a two-stage photolithography and lift-off process with Reactive Ion Etching (RIE). The resulting wedges may be used as field tip emitters.

Figure 6 is an illustration of a technique for creating a wedge emitter. The technique of J.G Flemming et al forms wedge shaped emitters.

Figure 7 is an illustration of a prior art technique for creating microtip emitters. The technique of Li et al East China Normal University utilizes an oxidation and pattern-transfer process to form microtips.

Figure 8 is an illustration of an application for microtip emitters. Field Emission (FE) flat panel displays have been created using microtip emitters. FE flat panel displays incorporating prior art microtip emitters generally require separate formation processes for the emitter tip and the emitter device.

Each of the above methods involves a multi-step process that requires special process conditions and is expensive. Additionally, the above methods do not easily allow multiple emission structures to be aligned in arrays with reliable uniformity, or the formation of different emitter geometries using one process. Finally, the above designs for field emission electron emitters are complex physical implementations with multiple components, again leading to high manufacturing costs and unreliable performance. Field emission electron emitters have a number of potential uses that are rendered impractical by the high cost, inherently low yield and difficulty of single-crystal design and fabrication.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

Figure 1 is an illustration of a technique for creating microtip emitters.

Figure 2 is an illustration of a technique for creating microtips.

Figure 3 is an illustration of a technique for creating microtip emitters.

Figure 4 is an illustration of a technique for creating microtip emitters.

Figure 5 is an illustration of a technique for creating microtip emitters.

Figure 6 is an illustration of a technique for creating microtip emitters.

Figure 7 is an illustration of a technique for creating microtip emitters.

Figure 8 is an illustration of an application for microtip emitters.

Figure 9 is an illustration a field emission structure in an example of the invention.

Figure 10 illustrates an electrical configuration for a field emission microtip emitter in an example of the invention.

Figure 11 illustrates an electrical configuration for a field emission microtip emitter in an example of the invention.

Figures 12 -19 illustrate combined steps of a simplified process flow for forming an array of microtip emitters consistent with process 2300 of Figure 23.

Figure 20 illustrates patterned topographies on a substrate.

Figure 21 illustrates atomically sharp objects corresponding to the patterned topographies of Figure 20.

Figure 22 is a top view of atomically sharp objects corresponding to the patterned topographies of Figure 21.

Figure 23 is a flowchart of a process for creating field emission structures in an example of the invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Embodiments of a design for new design structures and simplified methods for forming field emission structures are described herein. In the following description, numerous specific details are provided. However, one skilled in the relevant art will recognize that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

Various operations will be described as multiple discrete steps performed in a manner that is most helpful in understanding the invention. However, the order in which the steps are described does not imply that the operations are order-dependent or that the order that steps are performed must be the order in which the steps are presented.

The above problems are solved by a simplified electron emission structure formed using standard semiconductor processes wherein a substrate is first prepared with a patterned topographical feature. At least one layer of a first material is then concurrently deposited on the substrate and etched to form an atomically sharp feature. At least one layer of a conductive emission material is then deposited over the atomically sharp feature. At least one layer of an insulating material is then deposited over the conductive emission material. A conductive bias layer is then deposited over the at least one layer of insulating material. A region of deposited layers is then removed to expose the atomically sharp feature. Finally, electrical connectivity is provided to elements of the electron emission structure.

In an embodiment of the invention, a field emission structure is formed on a substrate. In another embodiment of the invention, highly uniform atomically sharp emitter microtips are self-formed and self-aligned using a continuous deposition and etch process such as a High Density Plasma (HDP) process. In an embodiment of the invention, the field emission structure may be formed concurrently with other components using standard semiconductor fabrication techniques. In an embodiment of the invention, an emission enhancing material is incorporated in field emission electron emitter fabrication for enhanced performance. In yet another embodiment of the invention, field emission emitter fabrication is secondary to a primary fabrication process. In yet another embodiment of the invention, field emission emitter microtips are further conditioned after fabrication by processes such as, but not limited to, electro-polishing.

In one embodiment of the invention, each of a plurality of field emitters is individually addressed with an electrical connection. In another embodiment of the invention, an array of field emitters is electrically connected. In yet another embodiment of the invention, a plurality of field emitters is electrically connected to provide electrostatic charge dissipation. In yet another embodiment of the invention, a device incorporating field emitters is fabricated according to the field emitter fabrication techniques of the invention.

In an embodiment of the invention, a Field Emission Display (FED) is fabricated using the field emitters of the invention. In yet another embodiment of the invention, a current source is formed using the field emitters of the invention. In another embodiment of the invention, a voltage source is formed using the field emitters of the invention. In

yet another embodiment of the invention, an ion pump is formed using the field emitters of the invention. In yet another embodiment of the invention, a package-level interconnect device is formed using the field emitters of the invention. In still another embodiment of the invention, a silicon vacuum tube is formed using the field emitters of the invention. In another embodiment of the invention, a switch is formed using the field emitters of the invention.

Simplified Field Emission Structures Figures 9-11

Figure 9 is an illustration a field emission structure in an example of the invention. In one embodiment of the invention, a field emission electron emitter 900 is formed on a substrate 901. Substrate 901 is prepared with a patterned topographical feature 902. The substrate is generally anisotropic silicon but may be any suitable material. A significant feature of the present invention is that single-crystal material is not required as a component. The topographical feature 902 may be any geometric design having width, length and height chosen for the specified application. One inherent advantage of the present invention is the ability to combine different topographic features on the same substrate using conventional patterning techniques. The patterning technique may be any method whereby a topographic feature is produced on a substrate, but is generally a deposition process.

At least one layer of a first material 903 is deposited over the substrate 901 containing the topographic feature 902 using a concurrent etch and deposit process, such as High Density Plasma Chemical Vapor Deposition (HDP-CVD) for example, to form an atomically sharp feature over the topographical feature 902. The first material 903 may be a conductor, semiconductor or insulator depending on the application, but is generally an insulator, such as an oxide. The atomically sharp feature is a field emission tip or microtip of appropriate geometry for field emission.

Optionally, a layer of conductive emission material 904 may be deposited over the first material 903, if for example the first material is an insulator. The conductive emission material is any conductor with a low work function and high emissivity such as tungsten, molybdenum, or a diamond-like graphite film for example. In an embodiment of the invention, a layer of emission enhancing material 905, such as thoriated tungsten for example, is additionally deposited on the conductive layer 904.

At least one layer of insulating material 906 is deposited over the at least one layer of conductive material 904 and any additional layers such as 905 for example. The insulating layer 906 may be any insulating material suitable for the application, but is generally an oxide of silicon.

A layer of conductive bias material 907 is deposited over the at least one layer of insulating material 905. The conductive bias layer may be any conductive material suitable for the application, but is generally aluminum or another common semiconductor connecting material. The conductive bias material 907 provides an electrical bias plane to the microtip emitter 900.

Deposited layers of material such as conductive bias material 907 and insulating material 906 are removed in a region 908 to expose the conductive material 904. The material removal process may be any method compatible with semiconductor fabrication, but is generally a mask and etch process.

An electrical connection 909 is provided to elements of the emission structure. As depicted in Figure 9, electrical connection 909 may be to conductive bias material 907, to conductive material 904 or to substrate 901.

Figure 10 illustrates an electrical configuration for a field emission microtip emitter in an example of the invention. A field emission electron emitter, such as 900 of Fig. 9, is depicted with a potential voltage 1010 across the conductive bias material 907 and the substrate 901.

Figure 11 illustrates an electrical configuration for a field emission microtip emitter in an example of the invention. A field emission electron emitter 900 is depicted with a potential voltage 1110 across the conductive bias material 907 and the conductive material 904.

Simplified Method for Forming Field Emission Structures Figures 12-23

Figure 23 is a flowchart of a process for creating field emission structures in an example of the invention. Process 2300 of Fig 23 begins in step 2310. Figures 12 -19 illustrate combined steps of a simplified process flow for forming an array of field emission microtip emitters consistent with process 2300 of Figure 23. Numbered elements of Figures 12-19 are carried though since the diagrams represent a process flow operating on the same elements. Figures 12-19 do not describe all possible process steps for

creating field emission electron emitters as contemplated by the present invention and are not exclusive of additional or optional steps.

Figure 12 is a top view of a patterned topographical feature. Figure 12 contains a substrate 1201 and a patterned topographical feature 1202. Figure 13 is a side view of a patterned topographic feature corresponding to Figure 12. Figure 13 contains a substrate 1201 and patterned topographical feature 1202.

Substrate 1201 is prepared with a patterned topographical feature 1202 in step 2310. In an alternative embodiment of the invention, step 2310 includes providing electrical connections on the substrate.

Figure 14 is a top view of an atomically sharp feature deposited with a conductive layer. Figure 14 contains an atomically sharp feature 1403 and a conductive layer 1404. Figure 15 is a side view of an atomically sharp feature deposited with a conductive layer corresponding to Figure 14. Figure 15 contains a substrate 1201, a patterned topographical feature 1202, an atomically sharp feature 1403, and a conductive layer 1404. A layer of a first material is concurrently deposited and etched to form an atomically sharp feature 1403 in step 2320. The first material may be a conductor, insulator or semiconductor material. The size, spacing and minimum height of the atomically sharp feature 1403 is determined by the shape of the patterned topographical feature 1202. A conductive material 1404 may optionally be deposited over the atomically sharp feature 1403 in step 2330.

Figure 16 is a top view of a conductive bias layer. Figure 16 contains a conductive bias layer 1607. Figure 17 is a side view of a conductive bias layer corresponding to Figure 16. Figure 17 contains a substrate 1201, a patterned topographical feature 1202, an atomically sharp feature 1403, a conductive layer 1404, an insulating layer 1706 and a conductive bias layer 1607. Insulating layer 1706 is deposited over the conductive layer 1404 in step 2340. Conductive bias layer 1607 is deposited over insulating layer 1706 in step 2350.

Figure 18 is a top view of an array of field emission microtip emitters. Figure 18 contains a pattern of removed material 1808 exposing atomically sharp features 1403. Figure 19 is a side view of an array of field emission microtip emitters corresponding to Figure 18. Figure 19 contains a substrate 1201, a patterned topographical feature 1202, an atomically sharp feature 1403, a conductive layer 1404, an insulating layer 1706, a

conductive bias layer 1607 and a pattern of removed material 1808 exposing the atomically sharp feature 1403. Material is removed from regions 1808 to expose atomically sharp features in step 2360.

Finally, electrical connectivity is provided to elements of the electron emission structure in step 2370. In an embodiment of the invention, a simultaneous fabrication process forms electrically functional devices on the substrate 1201. An electrically functional device is a passive or active device such as a resistor, capacitor, inductor, diode, wire trace, transistor, Light Emitting Diode (LED), photoresistor, or any combination of such devices that may function as elements of an electrical circuit.

An advantage of the present invention is the trivial formation of atomically sharp objects of varying size and shape using inexpensive materials and standard semiconductor fabrication techniques. An atomically sharp object used as an emitter microtip has a sharp geometry that promotes the emission of particles. The invention allows a unique particle emission characteristic for each emitter application since the topography of the emitter microtip can be tailored by the underlying geometry of the topographic feature on the substrate. An HDP-CVD process creates predictable microtip geometry depending on the size, spacing and minimum height of the underlying topographic feature.

Figure 20 illustrates patterned topographies on a substrate. A substrate 2001 contains several patterned topographical features 2002. The topographical features 2002 illustrated in Figure 20 have varying sizes, shapes and heights.

Figure 21 illustrates atomically sharp objects corresponding to the patterned topographies of Figure 20. Deposition of material 2103 using an HDP-CVD process over the topographic features 2002 as in step 2320 of process 2300 produces atomically sharp objects of varying geometries.

Figure 22 is a top view of atomically sharp objects corresponding to the patterned topographies of Figure 21. Microtips 2202 are formed using HDP-CVD deposited material 2203. Each of the topographic features depicted in Figs 21-22 may be combined to form other microtip 2202 geometries. Therefore, an unlimited variety of field emission structures in addition to field emission microtip emitters may be created using the method of the invention.

The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the

precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. A method for constructing electron emission structures, the method comprising:
preparing a substrate with a patterned topographical feature;
depositing at least one layer of a first material over the substrate;
etching the layer of the first material from the substrate concurrent with the depositing of the layer of the first material to form an atomically sharp feature;
depositing at least one layer of insulating material over the layer of first material;
depositing a layer of conductive bias material over the layer of insulating material;
removing a region of deposited layers to expose the atomically sharp feature; and,
providing electrical connectivity to elements of the electron emission structure.

2. The method of claim 1 further comprising:
depositing at least one layer of conductive emission material over the atomically sharp feature.

3. The method of claim 1 wherein the first material is polysilicon.

4. The method of claim 2 wherein the providing electrical connectivity to elements of the electron emission structure comprises providing electrical connectivity to the conductive bias layer.

5. The method of claim 2 wherein the providing electrical connectivity to elements of the electron emission structure comprises providing electrical connectivity to the substrate.

6. The method of claim 1 wherein the preparing the substrate with the patterned topographical feature comprises depositing material on the substrate.

7. The method of claim 1 wherein the preparing the substrate with the patterned topographical feature comprises etching the substrate.

8. The method of claim 1 further comprising:

performing at least one additional concurrent semiconductor fabrication process.

9. The method of claim 2 wherein the conductive emission material has a low work function and high emissivity.

10. The method of claim 2 further comprising:
depositing a conductive emission-enhancing layer over the conductive emission layer.

11. The method of claim 1 wherein the exposed electron emission structure is conditioned for improved performance.

12. An electron emission structure comprising:
a substrate prepared with a patterned topographical feature;
at least one layer of a first material deposited over the substrate and concurrently etched from the substrate to form an atomically sharp feature on the patterned topographical feature;
at least one layer of insulating material deposited over the layer of first material;
a layer of conductive bias material deposited over the layer of insulating material;
a patterned region wherein deposited layers of material are removed to expose the atomically sharp feature; and,
an electrical connection to elements of the emission structure.

13. The electron emission structure of claim 12 further comprising:
at least one layer of conductive emission material deposited over the atomically sharp feature.

14. The electron emission structure of claim 12 wherein the electrical connection is to the conductive emission layer.

15. The electron emission structure of claim 12 wherein the electrical connection is to the substrate.

16. The electron emission structure of claim 12 wherein the electrical connection is area addressable.

17. The electron emission structure of claim 12 wherein the electrical connection is device addressable.

18. The electron emission structure of claim 12 wherein the patterned topographical feature is a third material deposited on the substrate.

19. The electron emission structure of claim 12 wherein the patterned topographical feature is etched from the substrate.

20. The electron emission structure of claim 12 wherein the substrate contains another electrically functional device.

21. The electron emission structure of claim 20 wherein the electrically functional device is passive.

22. The electron emission structure of claim 20 wherein the electrically functional device is active.

23. The electron emission structure of claim 12 wherein the at least one layer of first material is a conductive material with a low work function and high emissivity.

24. The electron emission structure of claim 12 wherein an emission enhancing layer is added to the first layer of material.

25. A device incorporating electron emission structures, the device comprising:
an external electrical connection providing connectivity external to the device;
an electron emission structure comprising:
a substrate prepared with a patterned topographical feature;

at least one layer of a first material deposited over the substrate and concurrently etched from the substrate to form an atomically sharp feature on the patterned topographical feature;

at least one layer of insulating material deposited over the first material;

a layer of conductive bias material deposited over the layer of insulating material;

a patterned region wherein deposited layers of material are removed to expose the atomically sharp feature; and,

an electrical connection to elements of the emission structure; and,

an electrical connection between the electron emission structure and the external electrical connection.

26. The device of claim 25 wherein the electron emission structure further comprises at least one layer of conductive emission material deposited over the atomically sharp feature.

27. The device of claim 25 wherein the device dissipates electrostatic charge.

28. The device of claim 25 wherein the device is a visual display.

29. The device of claim 25 wherein the device is a package level interconnect.

30. The device of claim 25 wherein the device is a switch.

31. The device of claim 25 wherein the device is a silicon vacuum tube.

32. The device of claim 25 wherein the device is an ion pump.

33. The device of claim 25 wherein the device is a voltage source.

34. The device of claim 25 wherein the device is current source.

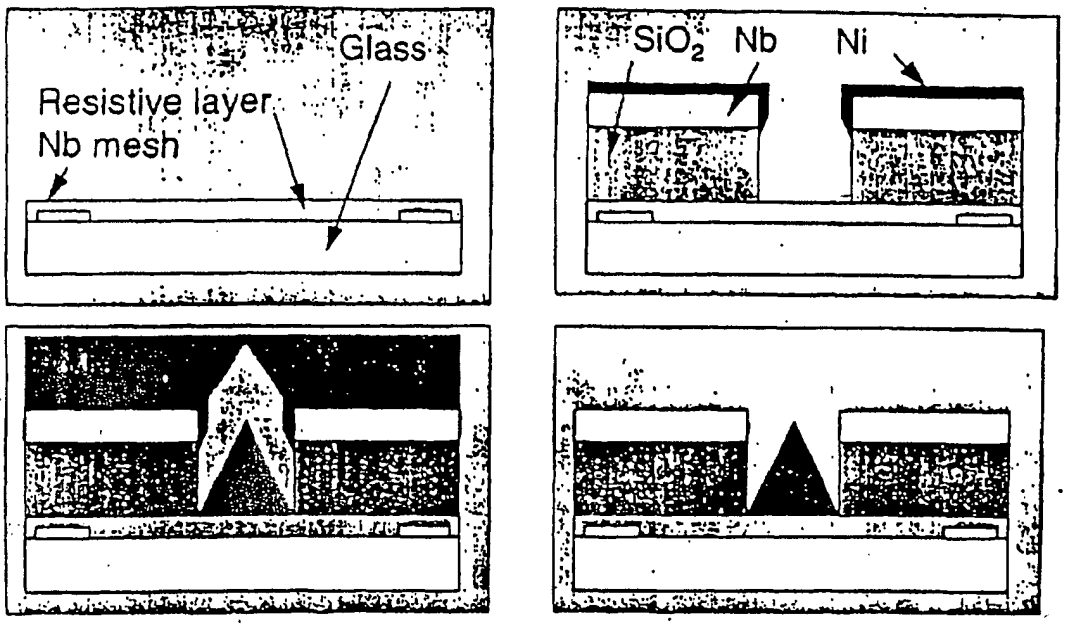


Fig 1

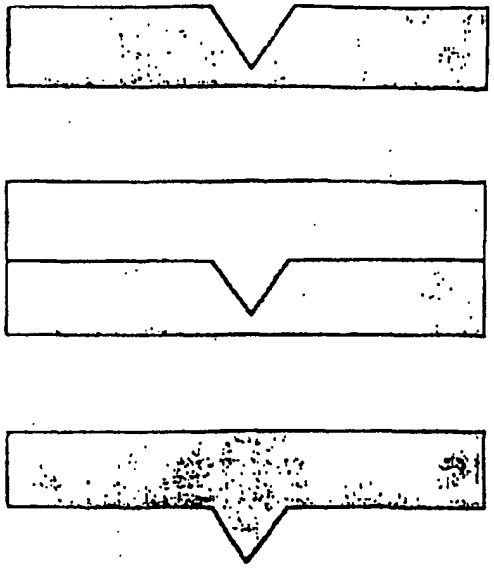


Fig 2

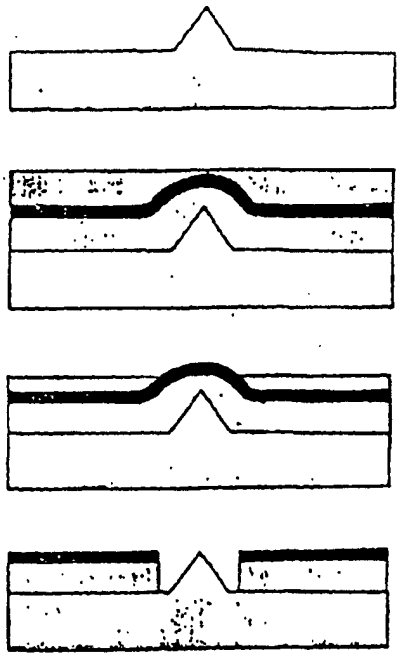


Fig 3

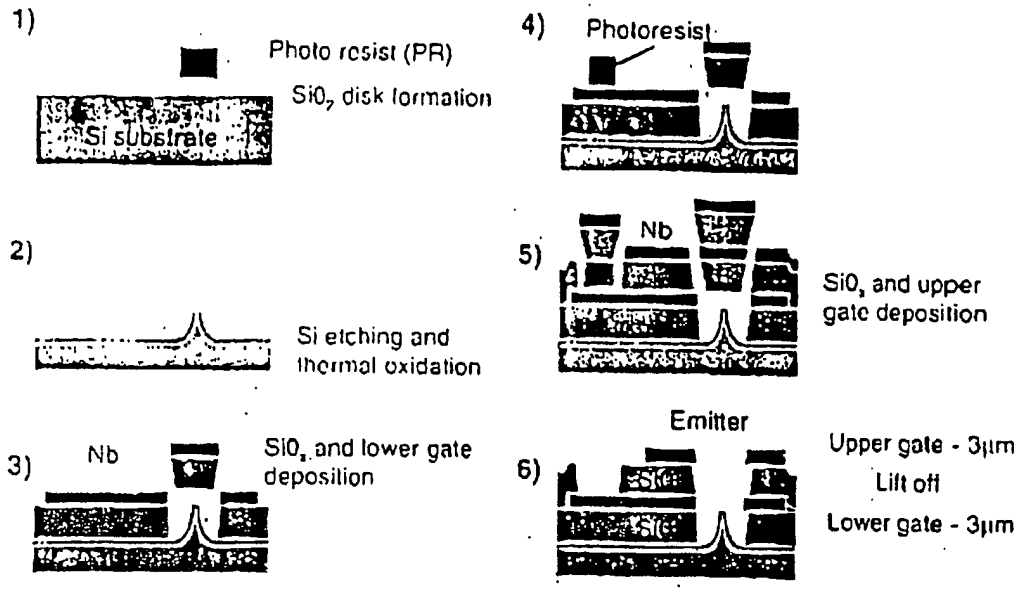


Fig 4

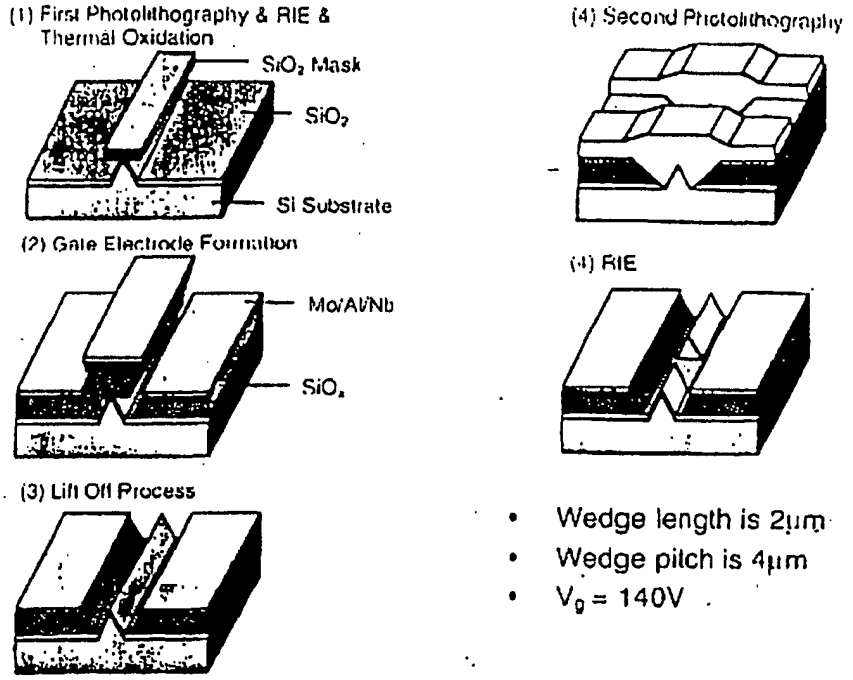


Fig 5.

1) Deposit and pattern oxide

2) Deposit and pattern grid

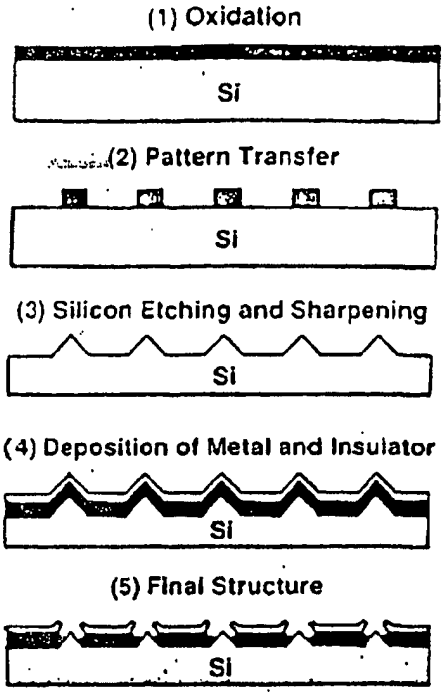
3) Deposit spacer oxide

4) Deposit conducting emitter layer

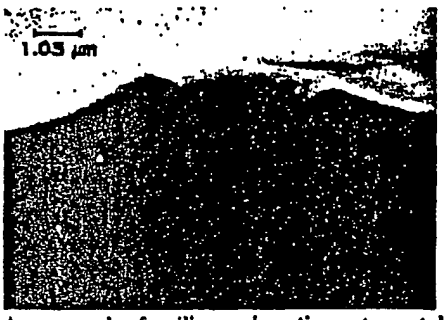
5) Form emitter wedge by RIE

6) Partially remove oxide separator

Fig 6

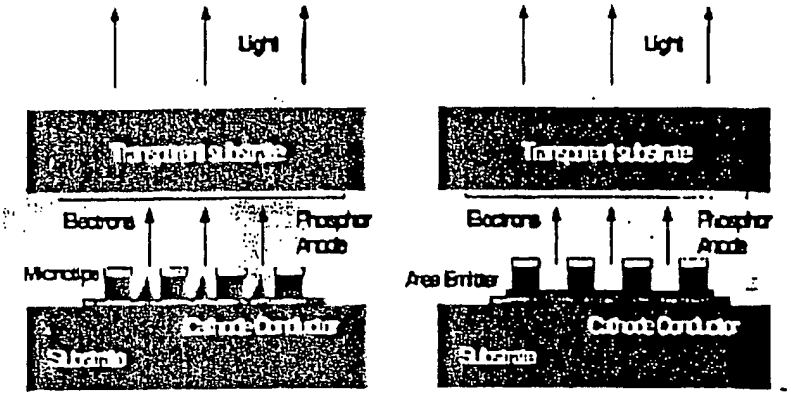


- **Potential Problems**
- Small spacing encourages leakage from cathode to grid
- Sharp grid edges encourages spurious emission grid to anode

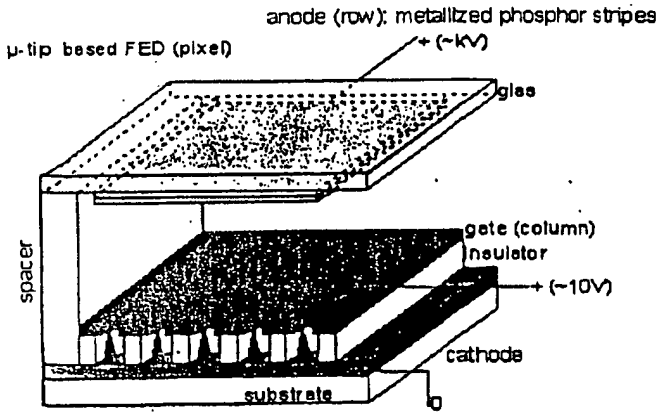


An example of a silicon micro tip; note unstable, asymmetric geometry.

Fig 7



Prior application of field effect emitters for FE flat panel display; formation of the tips was separate and problematic.



Another flat panel display example.

Fig 8

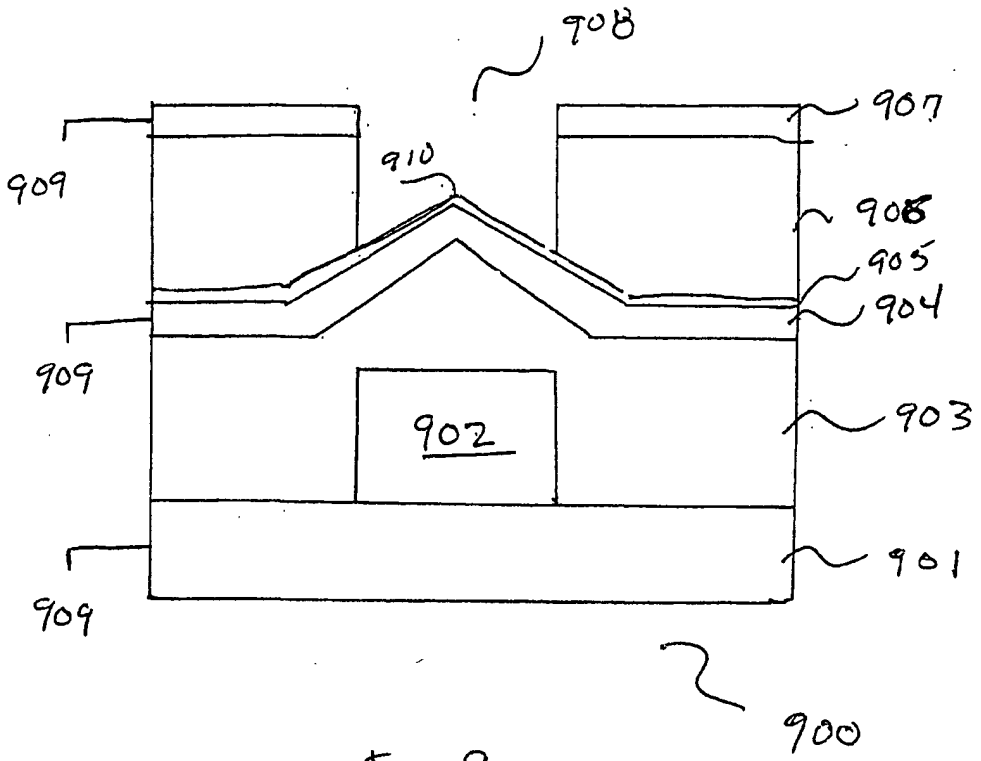


Fig 9

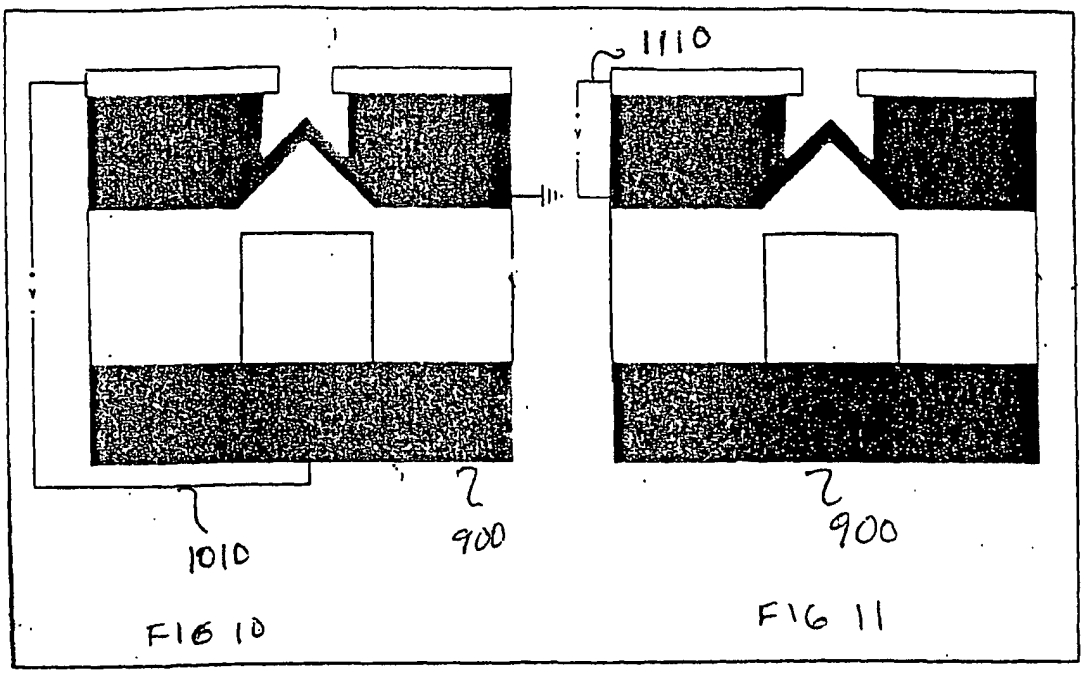
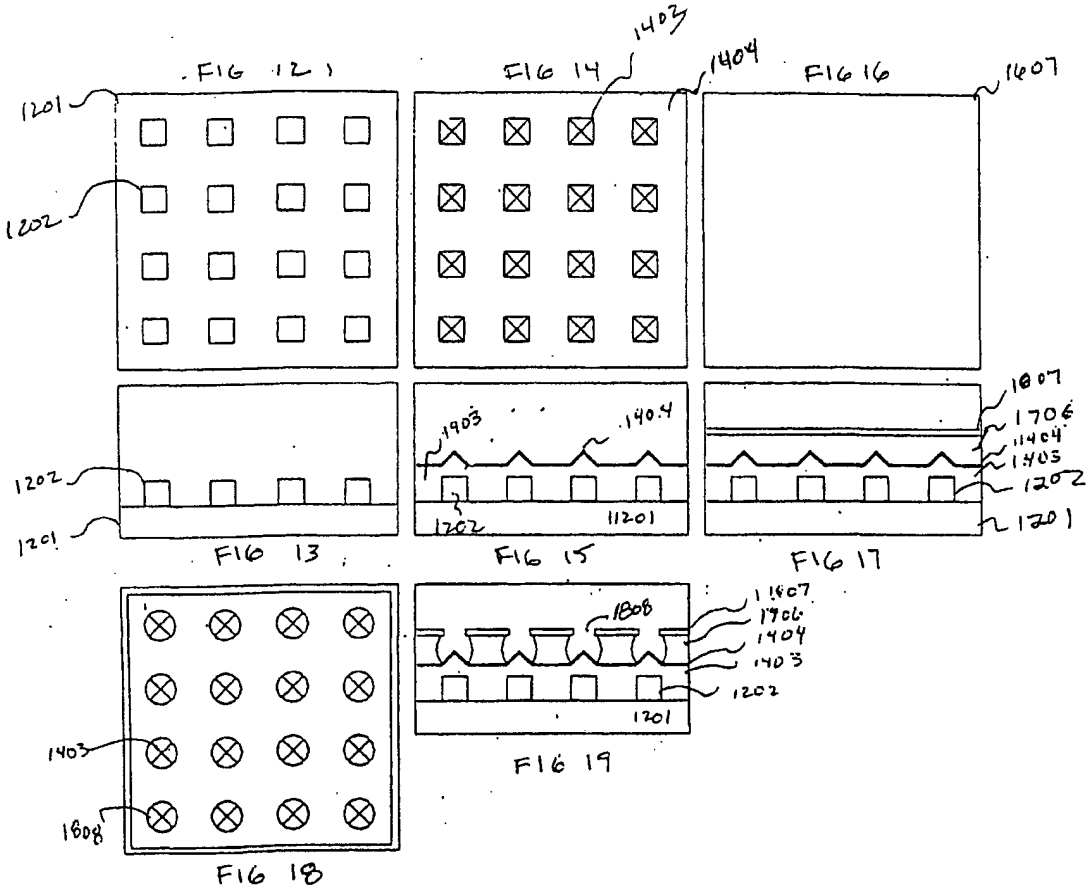


FIG 10

FIG 11



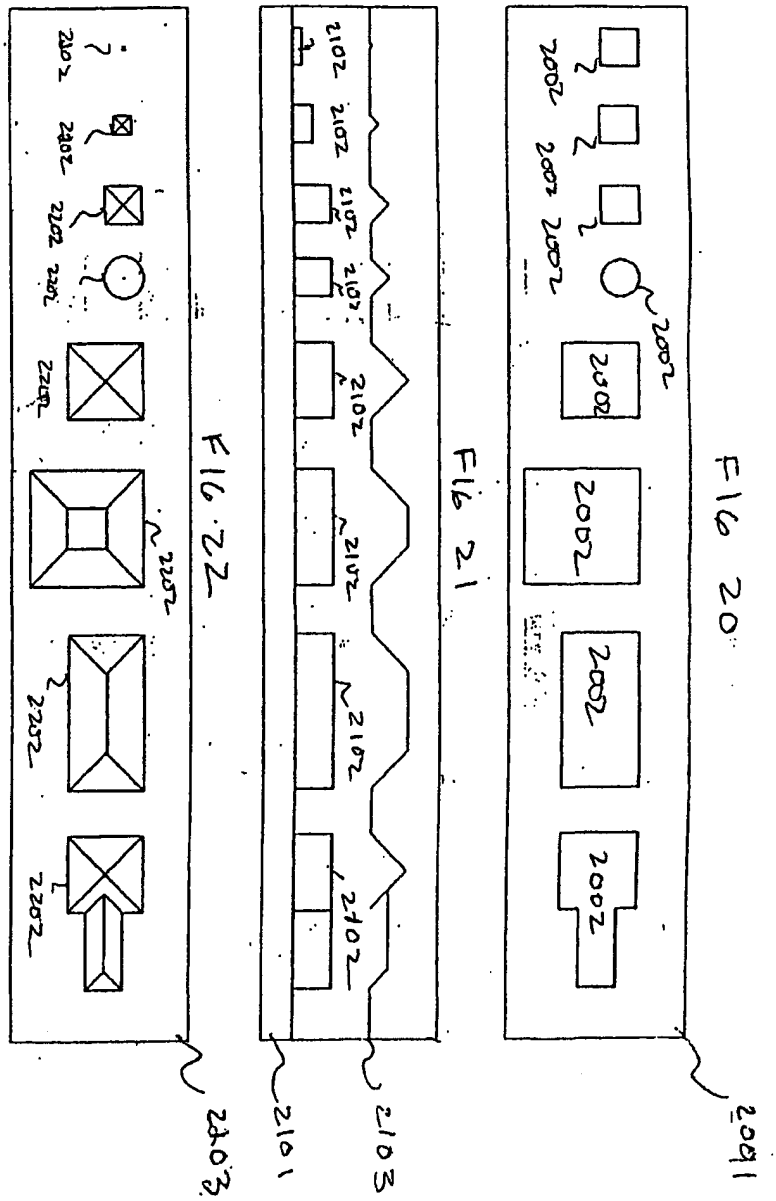


FIG 20

FIG 21

FIG 22

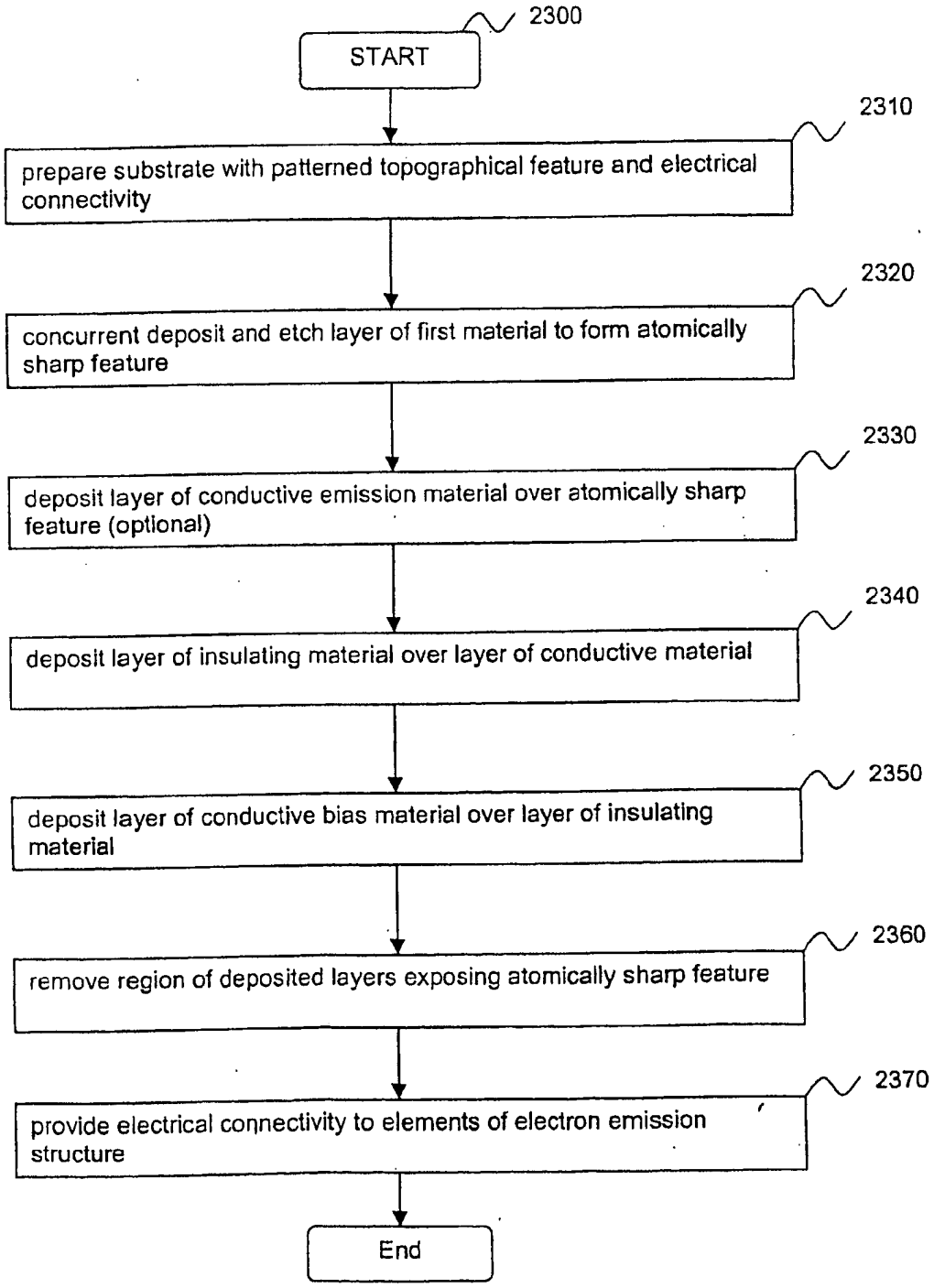

2300
START
2310
prepare substrate with patterned topographical feature and electrical connectivity
2320
concurrent deposit and etch layer of first material to form atomically sharp feature
2330
deposit layer of conductive emission material over atomically sharp feature (optional)
2340
deposit layer of insulating material over layer of conductive material
2350
deposit layer of conductive bias material over layer of insulating material
2360
remove region of deposited layers exposing atomically sharp feature
2370
provide electrical connectivity to elements of electron emission structure
End

FIG. 23

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(74) Agent: **MALLIE, Michael, J.**; Blakely Sokoloff Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

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(54) Title: NEW DESIGN STRUCTURES OF AND SIMPLIFIED METHODS FOR FORMING FIELD EMISSION MICROTIP ELECTRON EMITTERS

(57) Abstract: Electron emission structures formed using standard semiconductor processes on a substrate first prepared with a topographical feature are disclosed. At least one layer of a first material is concurrently deposited on the substrate and etched from the substrate to form an atomically sharp feature. An at least one layer of a second material is deposited over the atomically sharp feature. A conductive layer is deposited over the at least one layer of the second material. A selected area of material is removed from the conductive layer and the at least one layer of second material to expose the atomically sharp feature. Finally, electrical connectivity is provided to elements of the electron emission structure.

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, WPI Data, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 494 179 A (HORI YOSHIKAZU ET AL) 27 February 1996 (1996-02-27) claim 1	1
A	US 5 228 877 A (ALLAWAY MICHAEL J ET AL) 20 July 1993 (1993-07-20) claim 1	1

[ ] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
4 April 2003	11/04/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van den Bulcke, E

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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